CLAIMS

1. A method of forming a capacitor, the method comprising:

forming an insulating layer over a semiconductor substrate;

forming a contact plug in the insulating layer;

sequentially forming an etch stopping layer, a lower sacrificial oxide layer, and an upper sacrificial oxide layer over a surface of the semiconductor substrate having the contact plug;

patterning the lower and upper sacrificial oxide layers until a portion of the etch stopping layer over the contact plug is exposed to form a capacitor hole;

isotropically etching the lower sacrificial oxide layer to form an expanded capacitor hole therein;

etching the exposed portion of the etch stopping layer until an upper portion of the contact plug is exposed to form a final capacitor hole; and

cleaning the semiconductor substrate having the final capacitor hole to remove a native oxide film on the exposed upper portion of the contact plug.

2. The method of claim 1, wherein the etch stopping layer is made of nitride.

3. The method of claim 1, wherein the lower sacrificial oxide layer has a faster isotropic etching rate than the upper sacrificial oxide layer.

4. The method of claim 1, wherein the lower sacrificial oxide layer comprises a layer selected from the group consisting of a borophosphorsilicate glass (BPSG) layer, a phosphorsilicate glass (PSG) layer and an undoped silicate glass (USG) layer.

5. The method of claim 1, wherein the upper sacrificial oxide layer is made of plasma enhanced tetra-ethyl-ortho-silicate (PE-TEOS).

6. The method of claim 1, wherein the expanded capacitor hole is formed by wet-etching an exposed portion of the lower sacrificial oxide film in the capacitor hole.

7. The method of claim 6, wherein the wet-etching is performed using a hydrofluoric acid.

8. The method of claim 1, further comprising:

forming a conductive layer over the surface of the semiconductor substrate having the cleaned capacitor hole;

selectively removing a portion of the conductive layer over the upper sacrificial oxide layer to form a lower electrode in the cleaned capacitor hole; and

sequentially forming a dielectric layer and an upper electrode over a surface of the semiconductor substrate having the lower electrode.

9. The method of claim 8, wherein the conductive layer is conformally formed according to a step difference of the cleaned capacitor hole, and the lower electrode has a cylindrical shape in cross-section.

10. The method of claim 9, further comprising selectively removing the lower and upper sacrificial oxide layers to expose an outside wall of the lower electrode prior to formation of the dielectric layer and the upper electrode.

11. The method of claim 8, wherein the conductive layer is formed to fill the cleaned capacitor hole, and the lower electrode has a box shape in cross-section.

12. The method of claim 11, further comprising selectively removing the lower and upper sacrificial oxide layers to expose an outside wall of the lower electrode prior to formation of the dielectric layer and the upper electrode.

13. The method of claim 1, wherein cleaning the semiconductor substrate having the final capacitor hole is performed only to remove a native oxide film on the exposed upper portion of the contact plug so that cleaning process time can be reduced and the formation of an electrical bridge between the lower electrodes can be prevented.

14. The method of claim 1, wherein isotropically etching the lower sacrificial oxide layer is performed before etching the exposed portion of the etch stopping layer.

15. The method of claim 1, wherein etching the exposed portion of the etch stopping layer comprises exposing a portion of the insulating layer adjacent to the contact plug.

16. A semiconductor device formed by a process comprising:

forming an insulating layer over a semiconductor substrate;

forming a contact plug penetrating the insulating layer;

sequentially forming an etch stopping layer, a lower sacrificial oxide layer, and an upper sacrificial oxide layer over a surface of the semiconductor substrate having the contact plug;

patterning the lower and upper sacrificial oxide layers until a portion of the etch stopping layer over the contact plug is exposed to form a capacitor hole;

isotropically etching the lower sacrificial oxide layer to form an expanded capacitor hole;

etching the exposed portion of the etch stopping layer until an upper portion of the contact plug is exposed to form a final capacitor hole therein;

cleaning the semiconductor substrate having the final capacitor hole to remove a native oxide film on the exposed upper portion of the contact plug;

forming a conductive layer over the surface of the semiconductor substrate having the cleaned capacitor hole;

selectively removing a portion of the conductive layer over the upper sacrificial oxide layer to form a lower electrode in the cleaned capacitor hole; and

sequentially forming a dielectric layer and an upper electrode over a surface of the semiconductor substrate having the lower electrode.

17. The semiconductor device of claim 16, wherein the etch stopping layer is made of nitride.

18. The semiconductor device of claim 16, wherein the lower sacrificial oxide layer has a faster isotropic etching rate than the upper sacrificial oxide layer.

19. The semiconductor device of claim 16, wherein the lower sacrificial oxide layer comprises a layer selected from the group consisting of a borophosphorsilicate glass

(BPSG) layer, a phosphorsilicate glass (PSG) layer and an undoped silicate glass (USG) layer.

20. The semiconductor device of claim 16, wherein the upper sacrificial oxide layer is made of plasma enhanced tetra-ethyl-ortho-silicate (PE-TEOS).

21. The semiconductor device of claim 16, wherein the expanded capacitor hole is formed by wet-etching an exposed portion of the lower sacrificial oxide film in the capacitor hole.

22. The semiconductor device of claim 21, wherein the wet-etching is performed using a hydrofluoric acid.

23. The method of claim 16, wherein isotropically etching the lower sacrificial oxide layer is performed before etching the exposed portion of the etch stopping layer.

24. The method of claim 16, wherein etching the exposed portion of the etch stopping layer comprises exposing a portion of the insulating layer adjacent to the contact plug.